ROHM TECHNICAL NOTE

Large Current External FET Controller Type Switching Regulators

Single-output Step-up, Negative Voltage, Step-down Switching Regulators (Controller type)

BD9300F/BD9300FV

● Description

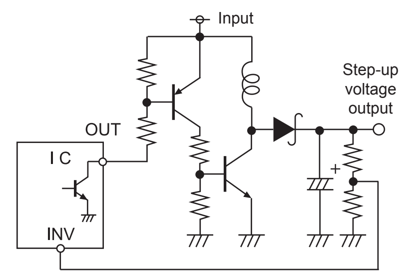
The BD9300F/FV 1-channel DC/DC Step-up, step-down, and inverting converter controller.
This IC has a wide input voltage range of 3.6 to 35 V, providing for a variety of applications. The pin assignment is similar to that of the BA9700, facilitating a space-saving application.

● Features

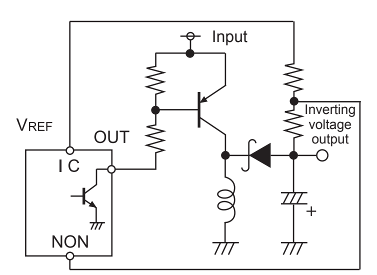
1) 1-channel PWM control DC/DC converter controller
2) High voltage input of 3.6 to 35 V
3) Reference voltage accuracy of ±1%
4) Oscillation frequency variable in the range of 20 to 800 kHz
5) Built-in UVLO (Under Voltage Lock Out) circuit and SCP (Short Circuit Prevention) circuit
6) Current in standby mode: 0 µA (typ.)
7) Switching external synchronization available (Slave operation)
8) SSOP-B14 Package (for BD9300FV) or SOP14 Package (for BD9300F)

● Applications

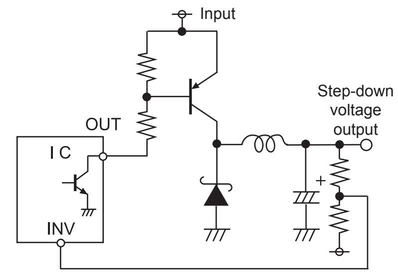
- TV, power supply for liquid crystal display TV, and backlight
- DSC, DVD, printer, DVD/DVD recorder, and other consumer products



Step-up voltage application



Inverting voltage application



Step-down voltage application

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ROHM CO., LTD.

● Absolute maximum ratings(Ta=25˚C)

Item	Symbol	Rating	Unit
Power supply voltage	Vcc	36	V
Power dissipation	Pd	400 *	mW
Operating temperature	Topr	–40 to +85	˚C
Storage temperature	Tstg	–55 to +125	˚C
Output current	Io	100 **	mA
Output voltage	Vo	36	V
Maximum junction temperature	Tjmax	125	˚C

* Reduce by 4 mW/˚C over 25˚C, when mounted on a glass epoxy PCB of 70mmX70mmX1.6mm)
** Should not exceed Pd-value.

● Recommended operating range (Ta=25˚C)

Item	Symbol	Limits			Unit
		Min	Typ	Max	
Power supply voltage	Vcc	3.6	12	35	V
Output sink current	I_O	–	–	30	mA
Output voltage	V_O	–	–	35	V
Timing capacitance	CT	33	–	1000	pF
Timing resistance	RT	5	–	100	kΩ
Oscillation frequency	Fosc	20	–	800	kHz

● Electrical characteristics (Unless otherwise specified, Ta=25˚C, V_{CC}=12V, CT=200pF, RT=20kΩ)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
[Reference voltage block]						
Reference voltage	V_{REF}	2.475	2.500	2.525	V	I_{REF}=1mA
Input stability	V_{DLI}	–	1.5	20	mV	Vcc=3.6 to 35V I_{REF}=1mA
Load stability	V_{DLD}	–	0.5	20	mV	I_{REF}=0 ~ 1mA
1/2 reference voltage	$1/2V_{REF}$	1.212	1.25	1.288	V	
[Triangular wave oscillator block]						
Oscillation frequency	F_{OSC}	165	220	275	kHz	
Charge mode threshold voltage	V_{OSC}^{+}	–	1.95	–	V	
Discharge mode threshold voltage	V_{OSC}^{-}	–	1.45	–	V	
Frequency variation	F_{DVO}	–	1	–	%	Vcc=3.6 to 35V
[Protection circuit block]						
Threshold voltage	V_{IT}	1.5	1.8	2.1	V	
Charge current	Iscp	–	7	11	μA	
[Rest period adjustment circuit block]						
Upper limit threshold voltage	Vt_H	2.05	–	–	V	Duty Cycle=0%
Lower limit threshold voltage	Vt_L	–	–	1.35	V	Duty Cycle=100%
Input bias current	Ibd	–	0.1	1	μA	DTC=1.5V
Latch mode charge current	Idtc	200	500	–	μA	DTC=0V
[Under voltage lock out block]						
Threshold voltage	V_{UT}	–	2.8	–	V	

○Not designed to be radiation-resistant.

● Electrical characteristics (Unless otherwise specified, Ta=25˚C, Vcc=12 V, CT=200pF, RT=20 kΩ)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
[Error amplifier block]						
Input bias current	I_{IB}	–	0.1	1	μA	
Open loop gain	AV	–	85	–	dB	Null AMP
Maximum output voltage	V_{OH}	2.3	2.5	–	V	
Minimum output voltage	V_{OL}	–	0.7	0.9	V	
Output sink current	I_{OI}	0.1	1	–	mA	V_{FB}=1.25V
Output source current	I_{OO}	40	70	–	μA	V_{FB}=1.25V
[Output block]						
Saturation voltage	V_{SAT}	–	1.0	1.4	V	Io=30mA
Leak current	I_{LEAK}	–	–	10	μA	OUT=35V
[Control block]						
CTL ON voltage	V_{ON}	2	–	–	V	
CTL OFF voltage	V_{OFF}	–	–	0.7	V	
CTL sink current	I_{CTL}	–	57	90	μA	V_{CTL}=5V
[Whole device]						
Standby current	I_{STB}	–	0	10	μA	V_{CTL}=0V
Average supply current	I_{CC}	–	1.2	2.4	mA	RT=VREF

○Not designed to be radiation-resistant.

● Measurement circuit diagram

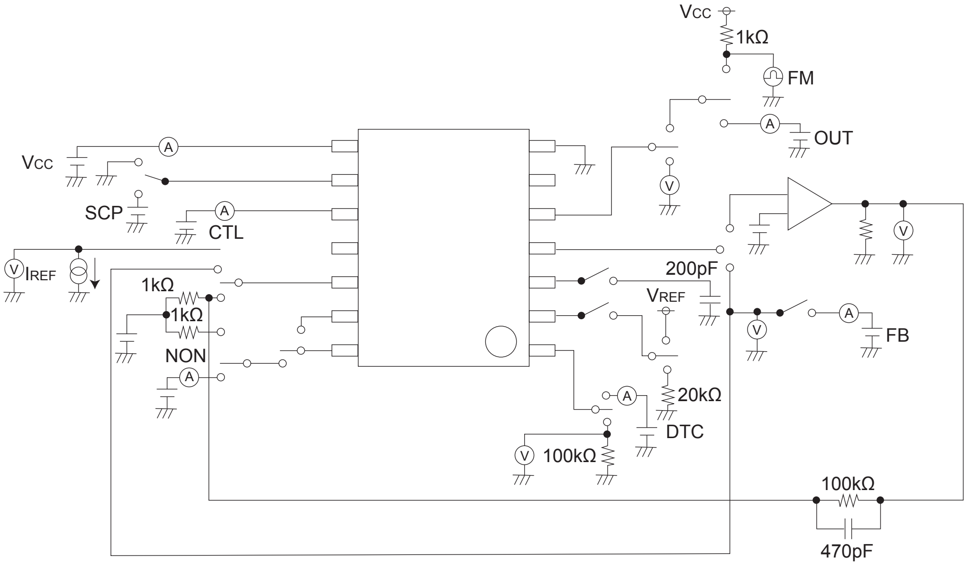


Fig. 1 Typical measurement circuit

● Reference characteristics data (Unless otherwise specified, Ta=25˚C)

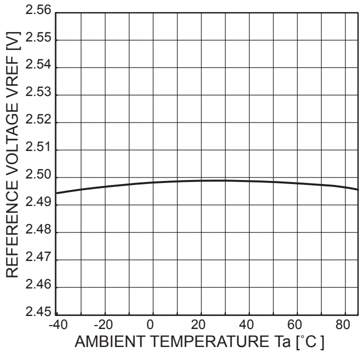


Fig.2 Reference voltage vs.
Ambient temperature

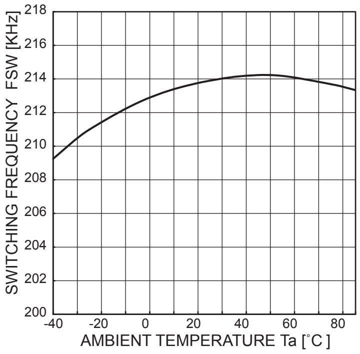


Fig.3 Switching frequency vs.
Ambient temperature

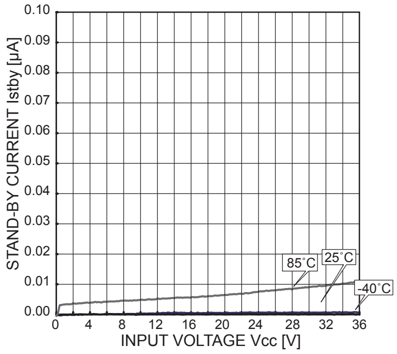


Fig.4 Standby current

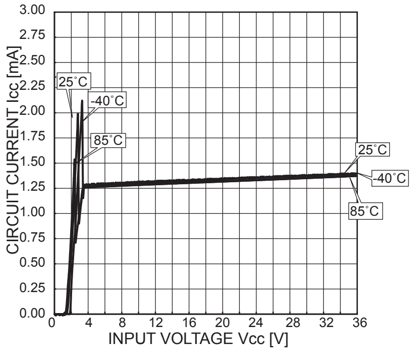


Fig.5 Circuit current

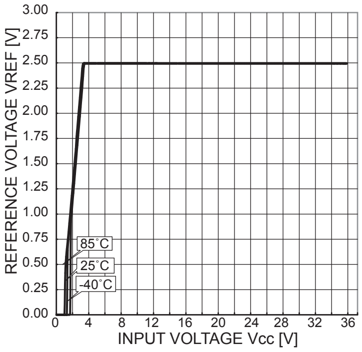


Fig.6 Reference voltage

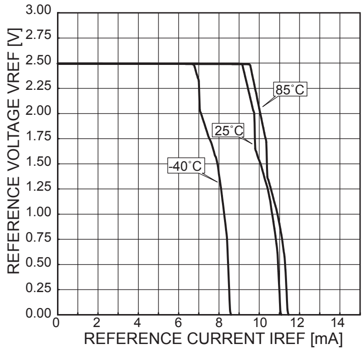


Fig.7 Reference voltage vs. Output current

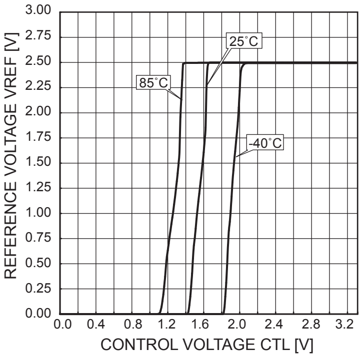


Fig.8 Control threshold voltage

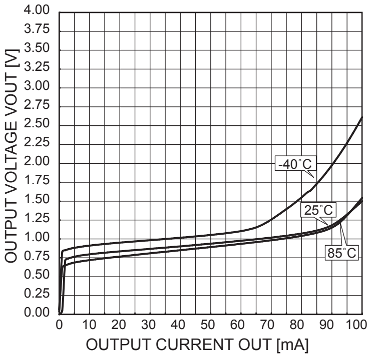


Fig.9 Output current capacitance

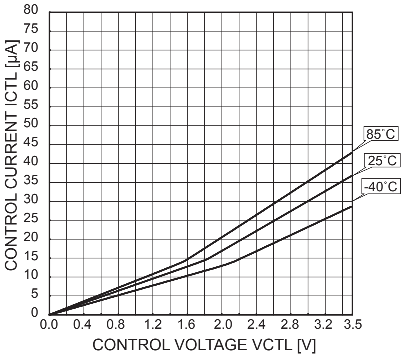
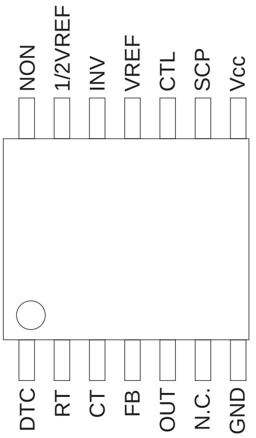


Fig.10 Control sink current

- Pin assignment



- Block diagram

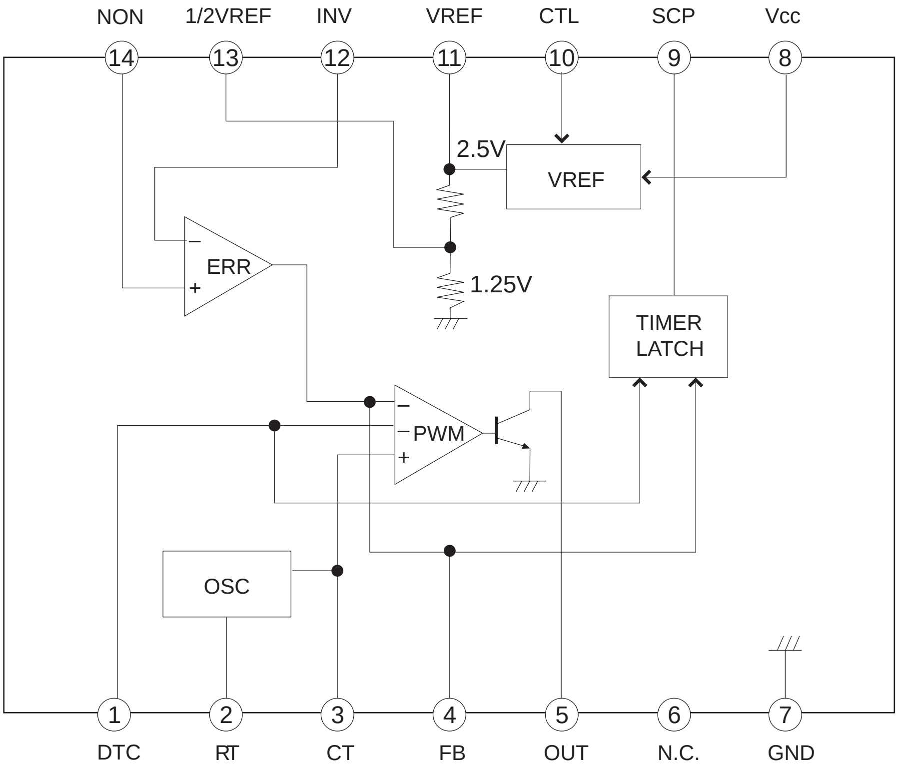


Fig. 11 Pin assignment / Block diagram

- Pin assignment and function

Pin No.	Pin name	Function
1	DTC	Rest period setting voltage input
2	RT	External timing resistance
3	CT	External timing capacitance
4	FB	Error amplifier output
5	OUT	PWM output (open collector)
6	N.C.	–
7	GND	Ground
8	Vcc	Power supply
9	SCP	External timer latch setting capacitance (Ground if not used)
10	CTL	Control input
11	VREF	Reference voltage output
12	INV	Inverting input for error amplifier
13	1/2VREF	1/2 reference voltage output
14	NON	Non-inverting input for error amplifier

● Description of operations

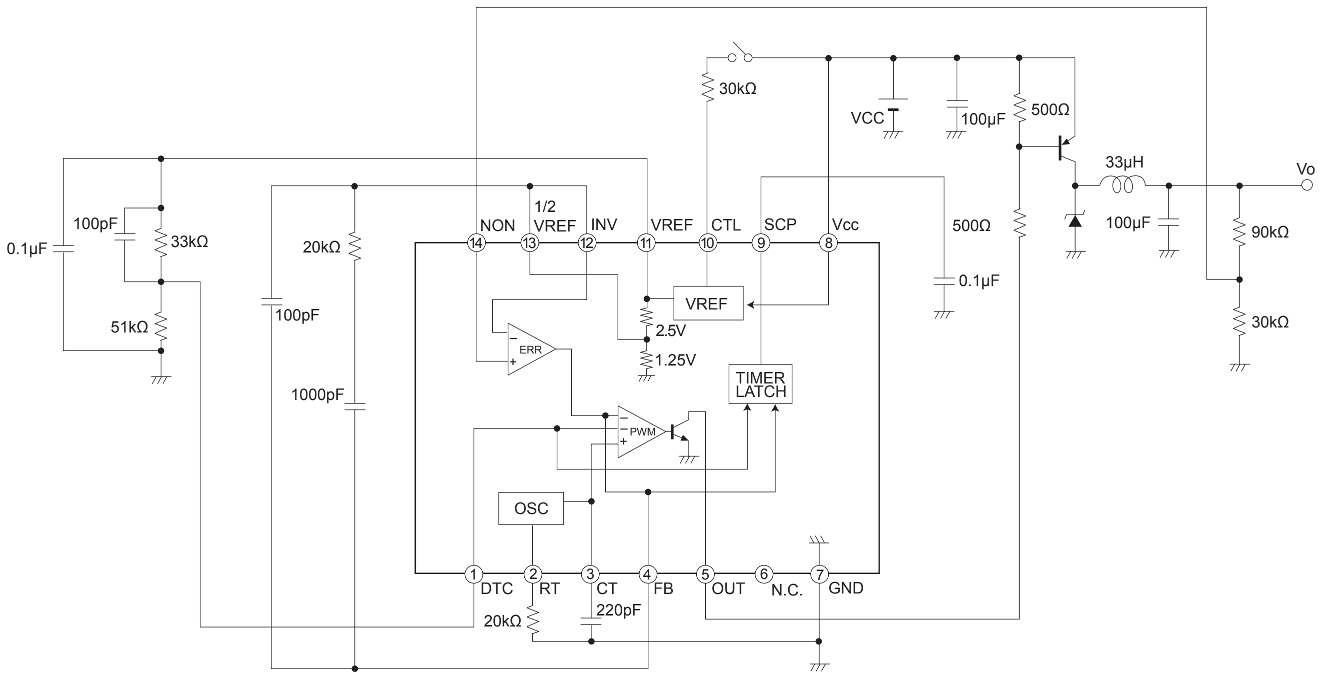


Fig. 12 Typical application circuit

VREF block

The VREF block is a block to output a reference voltage of 2.5 V (TYP), which is used as the operating power supply for all the Internal. The CTL pin is used to turn ON/OFF the reference voltage. Furthermore, this reference voltage has a current capacitance of 1 mA (MIN) or more, from which a high-accuracy reference voltage can be generated through dividing resistance.

ERRAMP block

The ERRAMP block is an error amplifier to amplify potential between the NON and the INV pins and then output a voltage. The FB pin output voltage determines the output pulse Duty. When the FB voltage reaches 1.95 V (TYP) or more, switching will be OFF (Duty=0%). When the FB voltage reaches 1.45 V (TYP) or less, the output NPN Tr will be FULL ON (Duty=100%).

OSC block

The OSC block is a block to determine the switching frequency through the RT and the CT pins. RT and CT voltages determine the triangular waveform.

TIMER LATCH block

The TIMER LATCH block is an output short circuit protection circuit to detect output short circuit when the output voltage from the FB pin of the error amplifier reaches 1 V (TYP) or less. When the FB voltage reaches 1 V (TYP) or less, the TIMER will starts operating to charge the SCP pin at a current capacitance of 7 μA (TYP). When the SCP voltage reaches 1.8 V (TYP), the LATCH will be activated to shut down the circuit.

PWM/Driver block

The PWM/Driver block is a PWM comparator to determine Duty value differences between output from the error amplifier and the oscillator triangular wave. The DTC voltage determines the maximum duty ratio. When the DTC voltage reaches 1.95 V (TYP), the switching OFF is activated. FULL ON will be activated when the DTC voltage reaches 1.45 V (TYP). The DTC voltage setting should be made through dividing resistance with the VREF block.

● Timing chart

· Basic operation

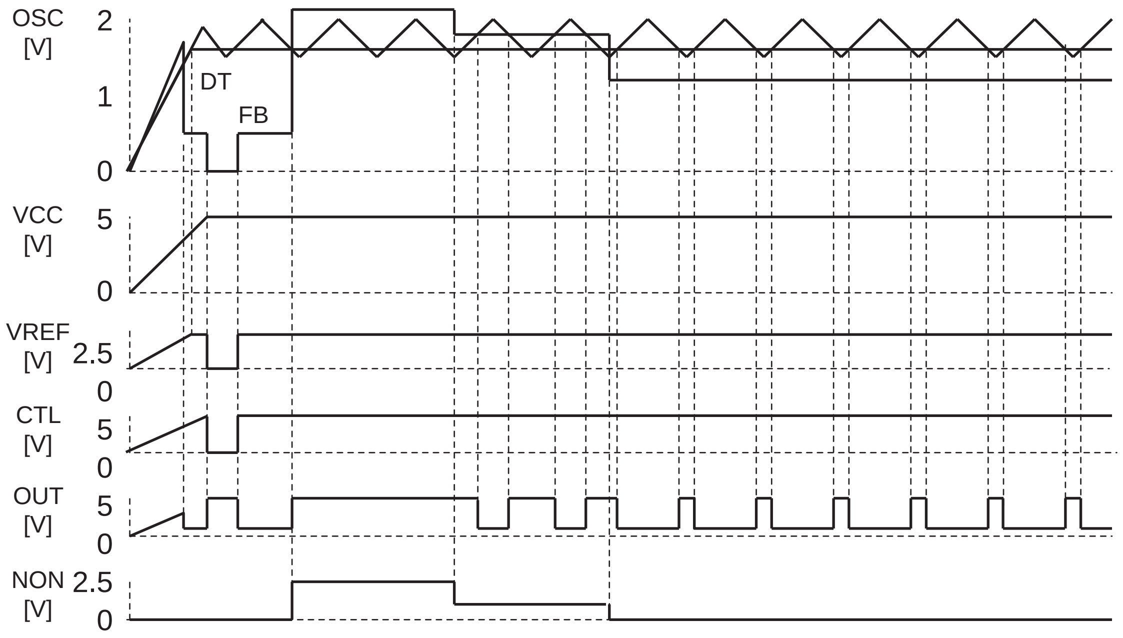


Fig. 13 Basic operation

· When the short circuit protection is activated

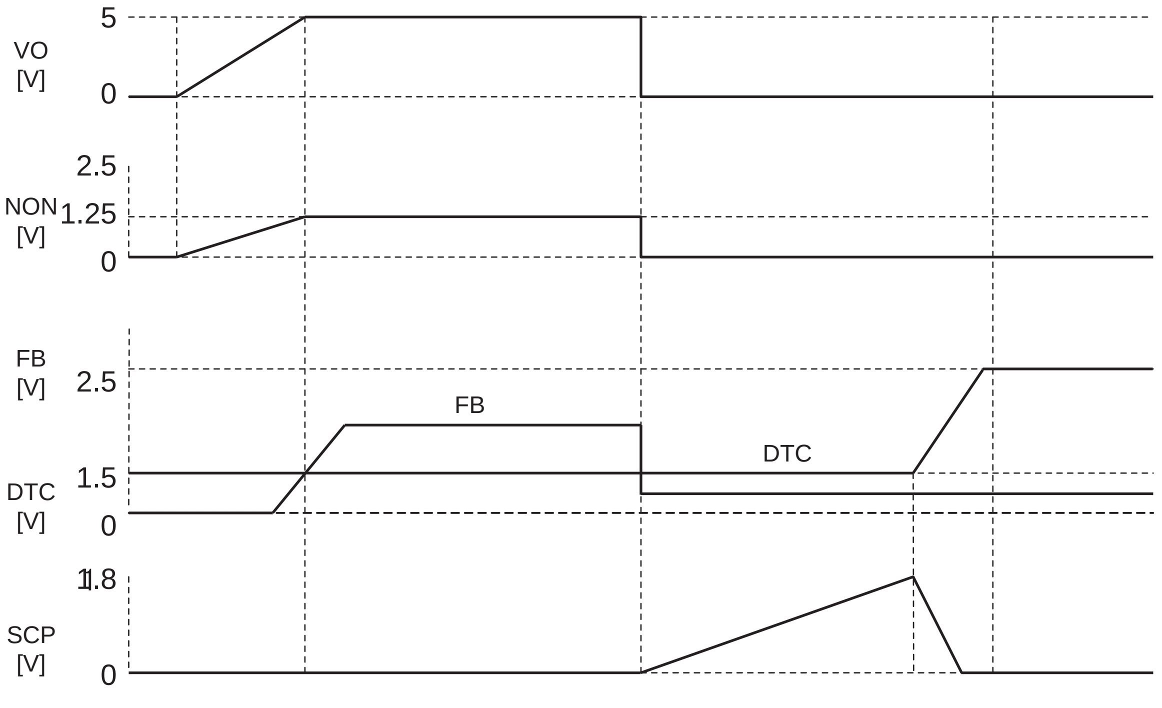


Fig. 14 Timing when the short circuit protection is activated

- External component setting procedure

(1) Design of feedback resistance constant

Set step-down, step-up, and inverting feedback resistance as shown below. Set resistance in the range of 1 kΩ to 330 kΩ. Setting the resistance to 1 kΩ or less will result in degraded power efficiency, while setting it to 330 kΩ or more will increase the offset voltage due to the input bias current of 0.1μA (TYP) of the error amplifier.

· Step-down voltage

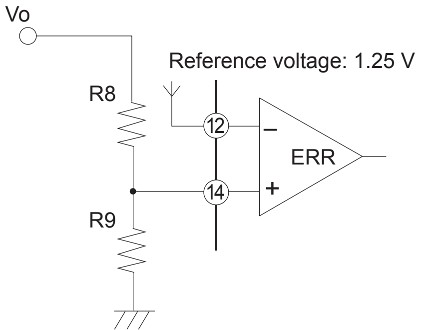


Fig. 15 Step-down voltage

· Step-up voltage

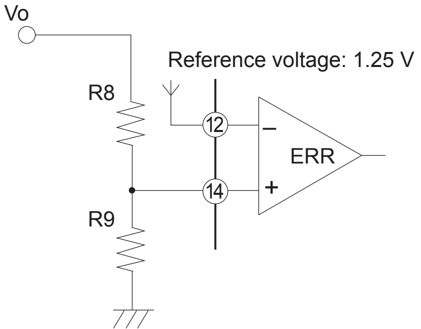


Fig.16 Step-up voltage

· Inverting voltage

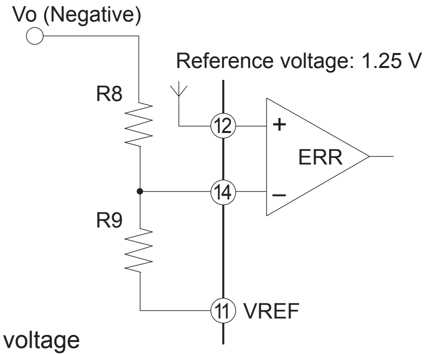


Fig. 17 Inverting voltage

$$Vo = \frac{R8+R9}{R9} \times 1.25\ [V]$$

$$Vo = \frac{R8+R9}{R9} \times 1.25\ [V]$$

$$Vo = 1.25\left(1-\frac{R8}{R9}\right)\ [V]$$

(2) Setting of oscillation frequency

Connecting a resistor and capacitor to the RT pin (pin 2) and the CT pin (pin 3) will set the triangular wave oscillation frequency. The RT determines the charge/discharge current to the capacitor. Referring to Fig. 18, set RT resistor and the CT capacitor. Recommended setting ranges are 5 to 100 kΩ for the CT resistor, 33 to 1000 pF for the CT capacitor, and 20 kHz to 800 kHz for the oscillation frequency. Any setting outside of these ranges may turn OFF switching, thus impairing the operation guarantee.

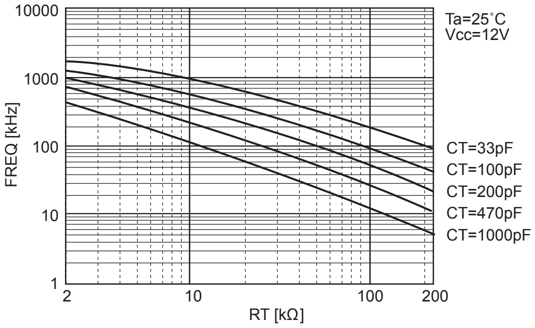


Fig. 18 RT/CT vs. Frequency

(3) Setting of DTC voltage

Applying the V_{DTC} voltage to the DTC pin (pin 1) will fix the maximum duty ratio.This will serve to prevent the power transistor (FET) from being FULL ON. Fig. 19 shows the relationship between the DTC voltage and the maximum duty ratio. Referring to this Figure, set the DTC voltage.Next, generate the V_{DTC} by dividing the V_{REF} voltage with resistance and then input the V_{DTC} in the DTC pin.

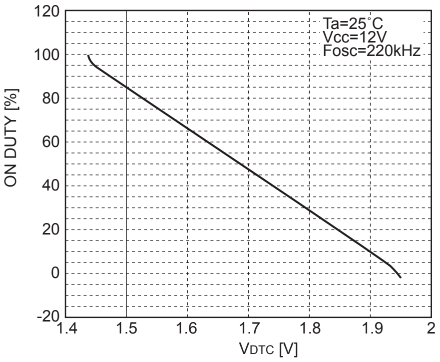


Fig. 19 DTC voltage vs. Maximum duty

Furthermore, the maximum duty ratio should be designed so as not to become a maximum duty for the normal use. The following section shows ranges for the normal use.

· Step-down voltage

$$ONDutyMAX = \frac{VOMAX}{VCCMIN}$$

· Step-up voltage

$$ONDutyMAX = \frac{VOMAX - VOMIN}{VOMAX}$$

· nverting voltage

$$ONDutyMAX = \frac{VOMAX}{VOMAX - VCCMIN}$$

(4) Setting of soft start time

Adding a capacitor to the DTC resistance divider will enable the soft start function activation.
The soft start function will be required to prevent an excessive increase in the coil current and overshoot of the output voltage, while in startup operation. Fig. 20 shows the relationship between the capacitor and the soft start time. Referring to this Figure, set the capacitor. It is recommended to set the capacitance value in the range of 0.01 to 10 µF. Setting the capacitance value to 0.01 µF or less, may cause overshoot to the output voltage, while setting it to 10 µF or more may cause an inverse current in the internal parasitic diode when the power supply is grounded, thus resulting in damage to the internal element.
the internal element.

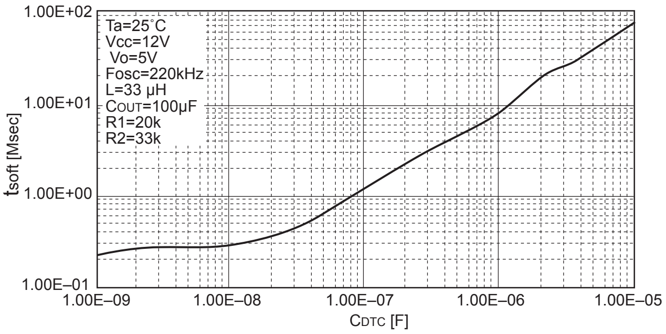


Fig. 20 Soft start capacitance vs. Delay time

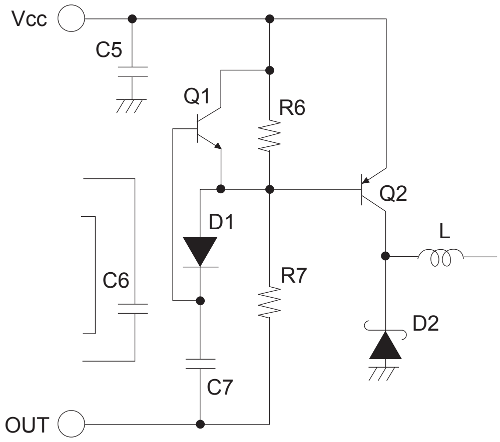


Fig. 21 ON/OFF peak circuit

Since the PNP Tr is generally slow in switching, in terms of the sat characteristics , the ON/OFF peak circuit is used as an acceleration circuit. The D1 and the C7 generate an ON peak current, while the Q1 and the C7 forms an OFF peak circuit.Set pull-up resistance to 510 Ω as a guide at VCC=12 V. It is recommended to set this resistance in the range of 100 kΩ to 10 kΩ. In order to make adjustment of the R6 and R7, however, pay attention of the points listed in table below.

NO.	Item	To reduce R6	To reduce R7
1	Efficiency	Degraded	Degraded
2	Tr Turn ON / Turn OFF	Faster Turn OFF	Faster Turn OFF
3	Switching frequency	Increasable	Increasable
4	Load current capacitance	Degraded	Degraded

Take 1000 pF as a guide for the C7 setting. If the ON/OFF peak currents are inadequate, increase the C7 capacitance value. It is recommended to set capacitance values in the range of 100 pF to 10000 pF. Setting the capacitance value to 10000 pF or more may increase the peak current and degrade the power efficiency.

(6) Phase compensation

Phase compensation setting procedure

The phase compensation setting procedure varies with the selection of output capacitors used for DC/DC converter application. In this connection, the following section describes the procedure by classifying into the two types. Furthermore, the application stability conditions are described in the Description section.

1. Application stability conditions
2. For output capacitors having high ESR, such as electrolytic capacitor
3. For output capacitors having low ESR, such as ceramic capacitor or OS-CON

1. Application stability conditions

The following section shows the stability conditions of negative feedback system.

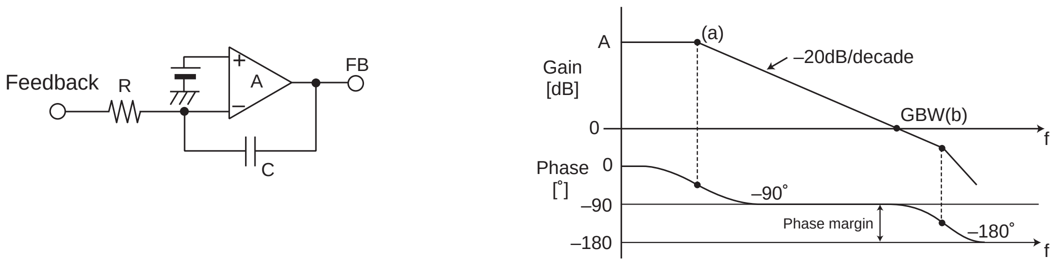
- DSC, DVD, printer, DVD/DVD recorder, and other consumer productsAt a 1 (0-dB) gain, the phase delay is 150° or less (i.e., the phase margin is 30° or more).

Furthermore, since the DC/DC converter application is sampled according to the switching frequency, GBW of the overall system should be set to 1/10 or less of the switching frequency. The following section summarizes the targeted characteristics of this application.

- DSC, DVD, printer, DVD/DVD recorder, and other consumer productsAt a 1 (0-dB) gain, the phase delay is 150° or less (i.e., the phase margin is 30° or more).
- DSC, DVD, printer, DVD/DVD recorder, and other consumer productsThe GBW (i.e., frequency at 0-dB gain) for this occasion is 1/10 or less of the switching frequency.

In other words, the responsiveness is determined with restrictions on the GBW. Consequently, in order to upgrade the responsiveness, higher switching frequency should be provided.

In order to ensure the stability through the phase compensation, a secondary phase delay (–180°) resulting from LC resonance should be canceled with a secondary phase lead (i.e., through inserting two phase leads).
Furthermore, the GBW (i.e., frequency at 1-dB gain) is determined according to phase compensation capacitance to be provided for the error amplifier. Consequently, in order to reduce the GBW, increase the capacitance value.



(1) Typical (sun) integrator (Low pass filter)

(2) Open loop characteristics of (mon) integrator

(a) point $f_a = \dfrac{1}{2\pi RCA}$ [Hz]

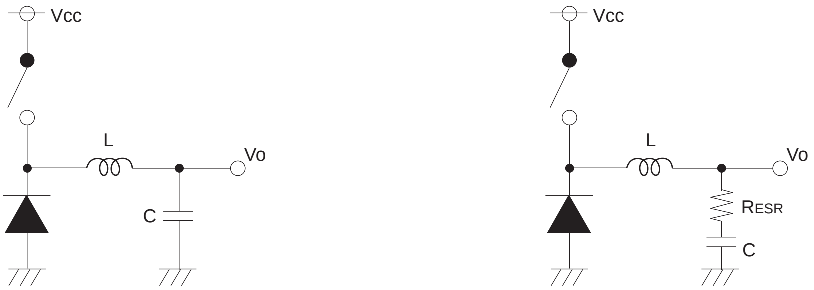
(b) point $f_b = \mathrm{GBW} = \dfrac{1}{2\pi RC}$ [Hz]

Fig. 22 Typical integrator characteristics

Since the error amplifier is provided with (sun) or (mon) phase compensation, the low pass filter is applied. In the case of the DC/DC converter application, the R becomes a parallel resistance of the feedback resistance.

2. For output capacitors having high ESR, such as aluminum electrolytic capacitor

For output capacitors having high ESR (i.e., several ohms), the phase compensation setting procedure becomes comparatively simple. Since the DC/DC converter application has a LC resonant circuit attached to the output, a –180˚ phase-delay occurs in that area. If ESR component is present there, however, a +90˚ phase-lead occurs to shift the phase delay to –90˚. Since the phase delay is desired to set within 150˚, this is a very effective method but has a demerit to increase the ripple component of the output voltage.



(3) LC resonant circuit

$$f_z = \frac{1}{2\pi\sqrt{LC}} \text{ [Hz]}$$

At this resonance point, a -180˚ phase-delay occurs.

(4) With ESR provided

$$f_z = \frac{1}{2\pi\sqrt{LC}} \text{ [Hz] : Resonance point}$$

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C} \text{ [Hz] : Phase lead}$$

A –90˚ phase-delay occurs.

* Same for the phase compensation of inverting and step-up voltages

Fig. 23 DC/DC converter output application

According to changes in phase characteristics due to the ESR, only one phase lead should be inserted. For this phase lead, select either of the methods shown below:

(5) Insert feedback resistance in the C.

$$\text{Phase lead: } f_z = \frac{1}{2\pi C1R1} \text{ [Hz]}$$

(6) Insert the R3 in integrator.

$$\text{Phase lead: } f_z = \frac{1}{2\pi C2R3} \text{ [Hz]}$$

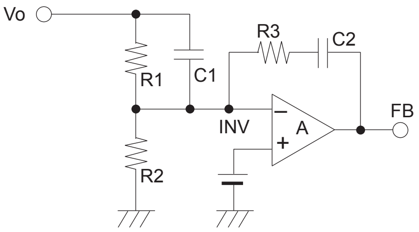
Fig. 24 Typical phase compensation circuit

To cancel the LC resonance, phase lead frequency should be set close to the LC resonant frequency.

3. For output capacitors having low ESR, such as a ceramic capacitor or OS-CON

   In order to use capacitors having low ESR (i.e., several tens of mW), two phase-leads should be inserted so that a – 180˚ phase-delay, due to LC resonance, will be compensated. The following section shows a typical phase compensation procedure.

   · Phase compensation with secondary phase lead



$$\text{Phase lead: } f_{Z1} = \frac{1}{2\pi R1C1} \text{ [Hz]}$$

$$\text{Phase lead: } f_{Z2} = \frac{1}{2\pi R3C2} \text{ [Hz]}$$

$$\text{LC resonant frequency: } fr = \frac{1}{2\pi\sqrt{LC}} \text{ [Hz]}$$

Fig. 25 Typical circuit after secondary compensation circuit

For the settings of phase lead frequency, insert both of the phase leads close to the LC resonant frequency.

Phase compensation on the BD9300F/FV

For BD9300F/FV, since the error amplifier input is inverted to the normal input, the phase compensation procedure is slightly different. (The BD9300F/FV returns feedback to the NON pin.)

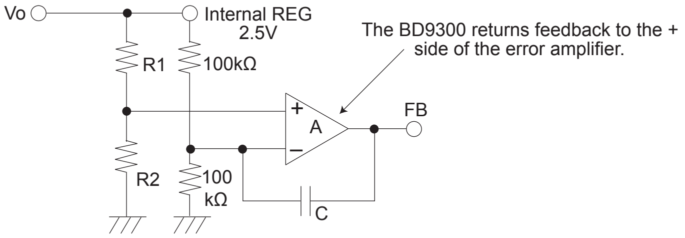


Fig. 26 Typical circuit after phase compensation on BD9300F/FV

The BD9300F/FV feeds back on the + side input and returns the phase compensation on the - side input. Consequently, resistance of the resistance divider being used to determine the reference voltage has influence on the frequency characteristics. (The BD9300F/FV has a 1/2 VREF pin to divide resistance by 100 kΩ.)

The following section shows the phase characteristics.

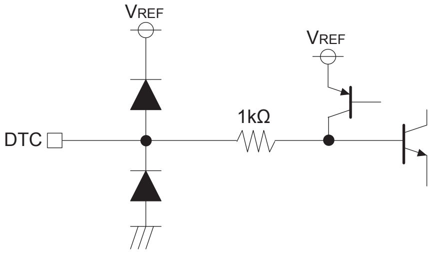
$$\text{Primary phase delay: } fp = \frac{1}{2\pi C \frac{100k\Omega}{2}(1+A)} \text{ [Hz], where A is approximately 80 dB.}$$

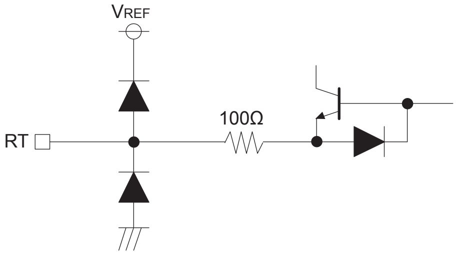
$$\text{Phase lead: } fz = \frac{1}{2\pi C \frac{100k\Omega}{2}} \text{ [Hz]}$$

As a result, inserting a phase compensation capacitor will cause phase lead component. If any further phase lead is required, add a capacitor in parallel with the R1.

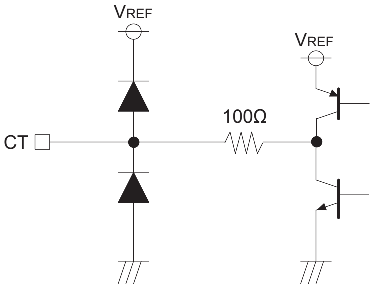
● Equivalent circuit

(1) DTC

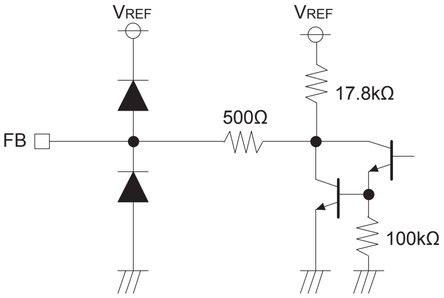




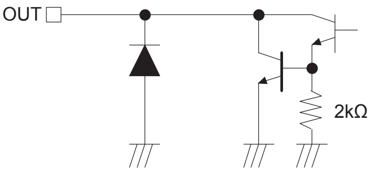
(3) CT



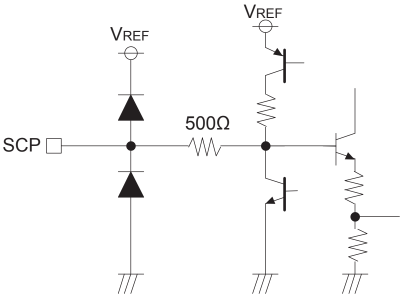
(4) FB



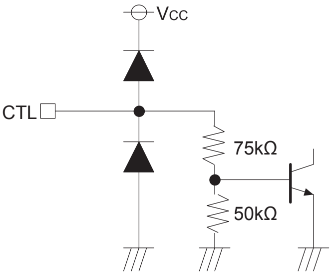
(5) OUT



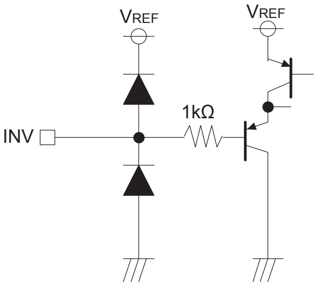
(9) SCP



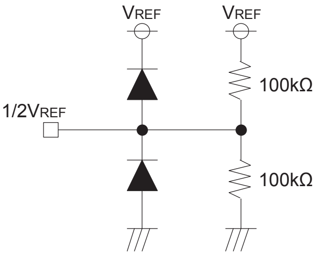
(10) CTL



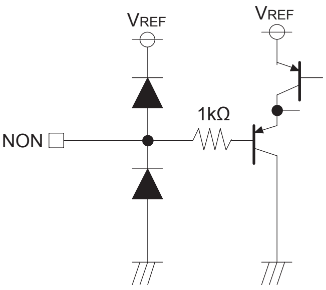
(12) INV



(13) 1/2VREF



(14) NON



● Cautions on use

1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2) GND potential

Ground-GND potential should maintain at the minimum ground voltage level. Furthermore, no terminals should be lower than the GND potential voltage including an electric transients.

3) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if positive and ground power supply terminals are reversed. The IC may also be damaged if pins are shorted together or are shorted to other circuitís power lines.

5) Operation in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to, or removing it from a jig or fixture, during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting and storing the IC.

7) IC pin input

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements to keep them isolated. PñN junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

○ When GND > Pin A and GND > Pin B, the PñN junction operates as a parasitic diode.

○ When Pin B > GND > Pin A, the PñN junction operates as a parasitic transistor.

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

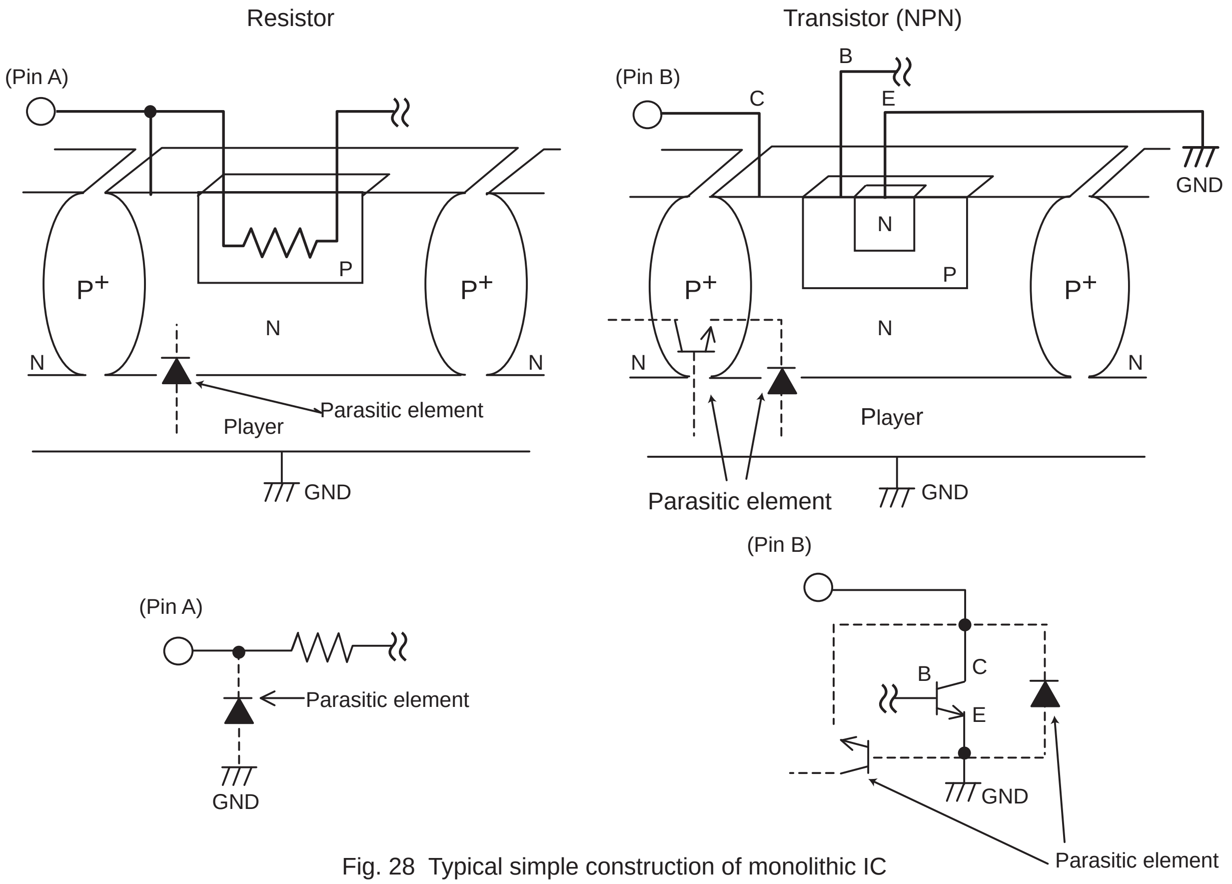


Fig. 28 Typical simple construction of monolithic IC

8) Ground wiring pattern

The power supply and ground lines must be as short and thick as possible to reduce line impedance. Fluctuating voltage on the power ground line may damage the device.

● Derating curve

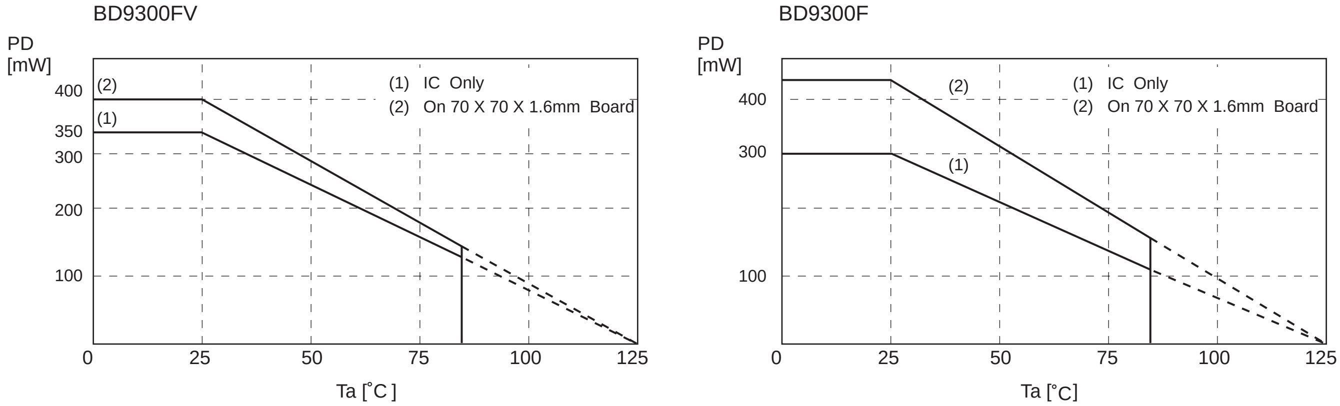


Fig. 29 Thermal derating characteristics

● Selection of order type

B D 9 3 0 0 F V – E 2

Product name

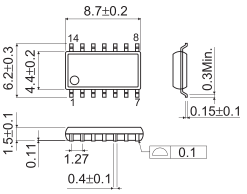
Package
FV:SSOP-B14
F :SOP14

Package/Forming specifications
E2 : Embossed carrier tape

● Package specifications

SOP14

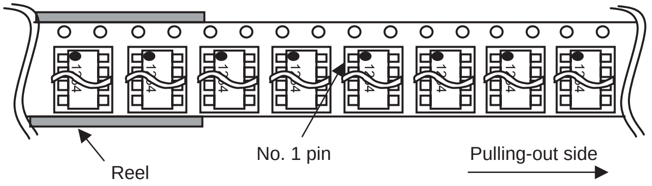
<Outline dimensions>



(Unit:mm)

<Package specifications>

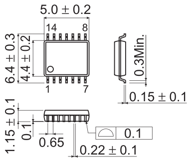
Package style	Embossed carrier tape
Q’ty per package	2500pcs
Packaging direction	E2 (When holding a reel by left hand and pulling out the tape by right hand, No. 1 pin appears in the upper left of the reel.)



*Orders are available in complete units only.

SSOP-B14

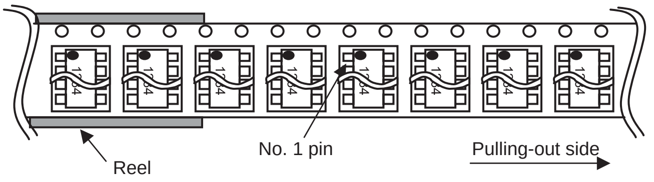
<Outline dimensions>



(Unit:mm)

<Package specifications>

Package style	Embossed carrier tape
Q’ty per package	2500pcs
Packaging direction	E2 (When holding a reel by left hand and pulling out the tape by right hand, No. 1 pin appears in the upper left of the reel.)



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21 Saiin Mizosaki-cho, Ukyo-ku, Kyoto
615-8585, Japan
TEL: +81-75-311-2121 FAX: +81-75-315-0172
URL http: // www. rohm. com

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